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[The Suppression of Phonon induced Noise in Niobium.. - Poelaert Peacock Rando \(1996\) \(Correct\) \(1 citation\)](#)
 follows similar work using an acoustic **mismatch model** [8,10,11] and is described in Appendix I. On
 or are reflected at the substrate-junction **interface**, or reach the base film after too many
 (table 2) for the substrate-buffer-Niobium **interface** cannot account for the dramatic attenuation of
astro.estec.esa.nl/pub/sciproj/poelaert_phonon1_JAP_01_03_96.ps.gz

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[Efficient support for IP over ATM - Hjalmtysson, Ramakrishnan \(Correct\)](#)
 and avoids the complexities caused by service **model mismatch**. 1. Introduction Modern communication
 it is becoming the de facto standard user network **interface**. The vast majority of new networking
 of new networking applications assume this **interface**. Consequently, ATM technology is increasingly
www.research.att.com/~gisli/papers/GH98.ATM98ws.sent.ps

[Compilation, Synthesis, and Simulation of Hardware Description.. - Cheng \(1998\) \(Correct\)](#)
 . 2 1.1.4 The **Model Mismatch** Problem .
 .6 1.3.1 Stacks As A Universal Procedure **Interface** .7 1.3.2 Structured
 7 1.3.1 Stacks As A Universal Procedure **Interface** The importance of this step is easy to
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[Embedding User Models in Intelligent Interfaces - Vadim Stefanuk Institute \(1997\) \(Correct\) \(2 citations\)](#)
situation and the given state of the User **Model**, **Mismatch** Registration` is designed to discover the
to the user. These services are taken from a **library** of available services. See [5] for a general
attached procedures are used for this purpose. A **library** of such procedures (some of them are shown in
www.cs.uni-sb.de/UM97/VS/ps/StefanukV.ps

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97 C.2.2 Comparing RTO Systems When Plant/**Model Mismatch** is Present .106 D Statistical Significance
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www.ualberta.ca/dept/chemeng/control/reports/fraser/thesis_gpffaff.pdf

[Statistical Estimation with 1/f-Type Prior Models - Dufour \(Correct\)](#)

two issues with the use of the 1=f models: **model mismatch** and parameter estimation. We show that the
Director, Graduate School Date Copy Deposited in **Library**: Reference Librarian Date Statistical
www.cdsp.neu.edu/info/students/rdufour/dufourMS.ps.gz

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[Measurement and Modeling of MOS Transistor Current Mismatch in.. - Eric Felt \(1994\)](#) (Correct) (1 citation)
 current mismatch and a new **transistor** current **mismatch model**. The new methodology is based on extracting
 Measurement and Modeling of MOS **Transistor** Current Mismatch in Analog IC's Eric Felt Amit
 presents a new methodology for measuring MOS **transistor** current mismatch and a new **transistor** current
ic.eecs.berkeley.edu/pub/Papers_Talks/Analog_Group/PostScript/ICCAD94_felt1.ps.Z

[Analog Integrated Circuits and Signal Processing.. - Systematic..](#) (Correct)
 is considered, and a new ve parameters MOS **mismatch model** is introduced. The current mismatch between
 Systematic Width-and-Length Dependent CMOS **Transistor** Mismatch Characterization and Simulation TERESA
 for characterizing the random component of **transistor** mismatch in CMOS technologies. The methodology
www.imse.cnm.es/~bernabe/kl_dec99.pdf

[An Asymptotically Constant, Linearly Bounded.. - Guardiani.. \(2000\)](#) (Correct)
 parameters. Second, applying a device level **mismatch model** to the statistical simulation of electronic
 and columns are ,representing parameter j for **transistor** i. The element represents the correlation
 between different parameters on different **transistors** is also taken to be zero.i. e.for and .
www.sigda.org/Archives/ProceedingArchives/Dac/Dac2000/papers/2000/dac00/htmlfiles/sun_sgi/.../pdffiles/01_4.pdf

[Evaluation Of The Substrate Noise Effect On Analog.. - Zinzius, Lauwers.. \(2000\)](#) (Correct)
 e#ect on the noise sensitivity. In addition a **mismatch model** was used #8#to see if device mismatch also
 topology through the bulk e#ect of the MOS **transistors** #4#Three e#ects can easily be located. The
 because they are already implemented in the **transistor** model #7#The body e#ect is in#uenced by the
www.imec.be/bandit/publications/ssmsd2000_Yann.pdf

[A 5-Parameter Mismatch Model for Short Channel MOS.. -..](#) (Correct)
 A 5-Parameter **Mismatch Model** for Short Channel MOS **Transistors**
 5-Parameter **Mismatch Model** for Short Channel MOS **Transistors** TeresaSerrano-Gotarredona and Bernab
 Abstract A new 5-parameter MOS **transistor mismatch model** is introduced capable of
www.imse.cnm.es/~bernabe/esscirc99.pdf

[A New Five-Parameter MOS Transistor Mismatch Model - Teresa Serrano-Gotarredona And](#) (Correct)
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 NO. 1, JANUARY 2000 37 A New Five-Parameter MOS **Transistor Mismatch Model** Teresa Serrano-Gotarredona and
 Abstract-A new five-parameter MOS **transistor mismatch model** is introduced capable of
www.imse.cnm.es/~bernabe/edl_jan00.pdf

[MOS Transistor Mismatch for High Accuracy Applications - Van der Plas..](#) (Correct)
 proportional to the mismatch (Pelgrom **mismatch model**)related through a technology constant. Also
 MOS **Transistor** Mismatch for High Accuracy Applications G. Van
 In this paper the matching behaviour of MOS **transistors** is analyzed for the realization of an
www.stw.nl/prorisc/prorisc99/proceedings/van_der_plas.pdf

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 Electron Device Letters, IEEE, Volume: 21, Issue: 1, Jan. 2000
 Pages:37 - 39

[\[Abstract\]](#) [\[PDF Full-Text \(104 KB\)\]](#) IEEE JNL
2 Disturbance and nonlinear Luenberger observers for estimating mechanical variables in permanent magnet synchronous motors under mechanical parameters uncertainties

Solsona, J.A.; Valla, M.I.;
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 Pages:407 - 412 vol.2

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4 Large-vocabulary continuous speech recognition: advances and applications

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Li Yu; Snelgrove, W.M.;

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[Abstract] [PDF Full-Text (1164 KB)] IEEE JNL

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van der Schaaf, T.W.; Brinkman, J.A.;

Systems, Man and Cybernetics, 1993. 'Systems Engineering in the Service of Humans', Conference Proceedings., International Conference on , 17-20 Oct. 1993
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11 Characterisation and modeling of mismatch in MOS transistors for precision analog design

Lakshmikumar, K.R.; Hadaway, R.A.; Copeland, M.A.;

Solid-State Circuits, IEEE Journal of , Volume: 21 , Issue: 6 , Dec 1986
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Relevance scale **1 Measurement and modeling of MOS transistor current mismatch in analog IC's**

Eric Felt, Amit Narayan, Alberto Sangiovanni-Vincentelli

November 1994

Proceedings of the 1994 IEEE/ACM international conference on Computer-aided design

Full text available: pdf(662.51 KB)

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This paper presents a new methodology for measuring MOS transistor current mismatch and a new transistor current mismatch model. The new methodology is based on extracting the mismatch information from a fully functional circuit rather than on probing individual devices; this extraction leads to more efficient and more accurate mismatch measurement. The new model characterizes the total mismatch as a sum of two components, one systematic and the other random. For our process, we attribute n ...

2 Working out usability: Linking surface error characteristics to root problems in user-based evaluation studies

Mark Springett

May 1998

Proceedings of the working conference on Advanced visual interfaces

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This paper reports a study of novice subjects using Word 5.1. for the Macintosh. In particular, user errors were analysed. The intention was to investigate the difficulty, that evaluators have in determining root error causes from surface characteristics. Errors made by subjects were examined and classified in phenotype and genotype categories[3]. An error was classified in a genotype category if it was felt that system had failed to support that particular user mental action. The utility of the ...

Keywords: action cycle, error studies, phenotypes/genotypes**3 Systematic design of a 14-bit 150-MS/s CMOS current-steering D/A converter**

G. Van der Plas, J. Vandenbussche, W. Daems, A. Van den Bosch, G. Gielen, W. Sansen

June 2000

Proceedings of the 37th conference on Design automation

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This paper presents a D/A converter with a 14-bit intrinsic linearity in 0.5µm CMOS technology, which has been designed using a systematic design methodology for current-steering D/A converters. A flexible architecture is proposed for which the design parameters are calculated using a performance-driven top-down design methodology. The layout of the regular structure typical for D/A converters is automatically generated. Measurement results are reported. Due to the systematic design m ...

4 Hierarchical statistical characterization of mixed-signal circuits using behavioral modeling

Eric Felt, Stefano Zanella, Carlo Guardiani, Alberto Sangiovanni-Vincentelli

January 1997

Proceedings of the 1996 IEEE/ACM international conference on Computer-aided design

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A methodology for hierarchical statistical circuit characterization which does not rely upon circuit-level Monte Carlo simulation is presented. The methodology uses principal component analysis, response surface methodology, and statistics to directly calculate the statistical distributions of higher-level parameters from the distributions of lower-level parameters. We have used the methodology to characterize a folded cascode operational amplifier and a phase-locked loop. This methodology permi ...

Keywords: statistical characterization, mixed-signal circuits, behavioral modeling

⁵ [Synthesis of manufacturable analog circuits](#)

Tamal Mukherjee, L. R. Carley, R. A. Rutenbar

November 1994

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We describe a synthesis system that takes operating range constraints and inter- and intra-circuit parametric manufacturing variations into account while designing a sized and biased analog circuit. Previous approaches to CAD for analog circuit synthesis have concentrated on nominal analog circuit design, and subsequent optimization of these circuits for statistical fluctuations and operating point ranges. Our approach simultaneously synthesizes and optimizes for operating and manufacturing ...

⁶ [Confidence intervals for univariate discrete-event simulation output using the Kalman filter](#)

Randall B. Howard, Mark A. Gallagher, Kenneth W. Bauer, Peter S. Maybeck

December 1992

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